CLAIMS

What is claimed is:

1. A multi-chips stacked package, comprising:

a substrate having an upper surface, a lower surface and an opening passing through the upper surface and the lower surface;

an upper chip having a first active surface and a first back surface wherein the upper chip is flipped over and attached to the upper surface of the substrate via a plurality of first electrically conductive bumps;

a lower chip accommodated in the opening and electrically connected to the first active surface of the upper chip through a plurality of second electrically conductive bumps;

a dam disposed on the upper surface of the substrate; and

a heat spreader attached to the first back surface of the upper chip and attached to the dam.

2. The multi-chips stacked package of claim 1, further comprising an adhesive layer interposed between the heat spreader and the first back surface of the upper chip.

3. The multi-chips stacked package of claim 2, wherein the adhesive layer is a thermally conductive epoxy.

4. The multi-chips stacked package of claim 1, wherein the dam is disposed at the periphery of the upper surface of the substrate and surrounds the upper chip.

5. The multi-chips stacked package of claim 4, wherein the dam is ring-like.

6. The multi-chips stacked package of claim 1, further comprising an encapsulation filled in a space enclosed by the heat spreader, the upper surface of the substrate

and the dam.

7. The multi-chips stacked package of claim 6, wherein the encapsulation comprises an underfill.

8. The multi-chips stacked package of claim 7, wherein the underfill encloses the upper chip, the lower chip, the first electrically conductive bumps and the second electrically conductive bumps, and covers the upper surface of the substrate.

9. The multi-chips stacked package of claim 7, wherein the underfill is connected to the upper surface of the substrate, the heat spreader and the dam.

10. The multi-chips stacked package of claim 1, wherein a material of the heat spreader comprises copper.

11. The multi-chips stacked package of claim 1, wherein a material of the heat spreader comprises aluminum.

12. The multi-chips stacked package of claim 1, wherein the heat spreader is a flat plate.

13. The multi-chips stacked package of claim 1, further comprising a plurality of solder balls formed on the lower surface of the substrate.

14. The multi-chips stacked package of claim 1, wherein the dam is an adhesive body.

15. The multi-chips stacked package of claim 1, wherein a material of the dam comprises epoxy.

16. The multi-chips stacked package of claim 15, wherein the material of the dam is selected from thermally conductive epoxy.

17. The multi-chips stacked package of claim 1, wherein the dam is formed in a

bar-like shape.

18. The multi-chips stacked package of claim 8, wherein the lower chip has a second back surface exposing out of the underfill.

19. The multi-chips stacked package of claim 1, wherein the heat spreader is a flat plate.

20. The multi-chips stacked package of claim 1, further comprising a plurality of solder balls formed on the lower surface of the substrate.

21. The multi-chips stacked package of claim 1, wherein the upper chip is larger than the lower chip in size.

22. A multi-chips stacked package, comprising:

a substrate having an upper surface and a lower surface;

an upper chip having a first active surface and a first back surface wherein the upper chip is flipped over and attached to the upper surface of the substrate via a plurality of first electrically conductive bumps;

a lower chip disposed above the upper surface of the substrate and electrically connected to the first active surface of the upper chip through a plurality of second electrically conductive bumps;

a dam disposed at the periphery of the upper surface of the substrate; and

a heat spreader attached to the first back surface of the upper chip and attached to the dam.

an underfill enclosing the upper chip, the lower chip, the first electrically conductive bumps and the second electrically conductive bumps, and covering the upper surface of the substrate.

23. The multi-chips stacked package of claim 22, wherein the first electrically conductive bump is larger than the second electrically conductive bump in height.